

Design A High-Resolution Δ - Σ ADC Using An 8-Bit Microcontroller

A simple integrating amplifier is combined with an MCU's analog peripherals to realize a 10-bit analog-to-digital converter.

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There are numerous methods of implementing delta-sigma (Δ - Σ) analog-to-digital converters (ADCs), and each has its own set of advantages and disadvantages. Some engineers employ complex systems to solve simple conversion problems, while others exploit simple circuits to handle difficult tasks. A deeper analysis of the basic circuit, however, can lead to some interesting low-cost alternatives. The fundamental Δ - Σ ADC model, described in this article, is an inexpensive design strategy. It requires a simple integrating amplifier and a microcontroller's analog peripherals to create a high-resolution converter.

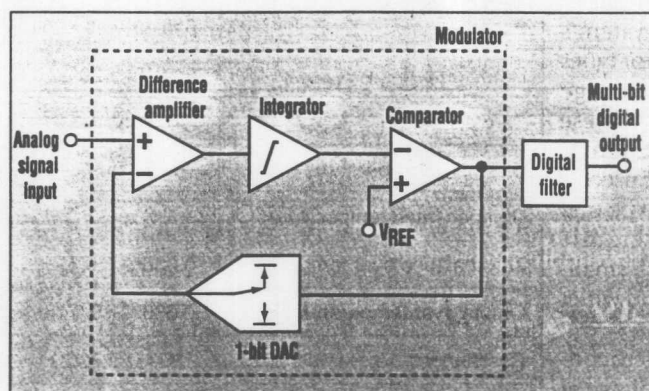
In this scheme, the conversion from analog to digital is performed with the internal-voltage reference, comparator, and two counters in the 8-bit microcontroller. These internal-microcontroller analog peripherals, along with the external integrator, are used to complete the implementation of a first-order modulator. This modulator is then combined with an output-digital filter, which also is implemented in the microcontroller unit, to complete the design. Consequently, the only components external to the microcontroller are an

op amp, two resistors, and a capacitor.

Until now, the microcontroller alone wasn't able to handle the Δ - Σ function, except for the digital-filter block. But, the recent addition of analog cells to the controller's silicon makes such an integrated solution possible.

Basically, the Δ - Σ ADC can be simply modeled with a modulator and a digital filter (Fig. 1). The modulator part of this ADC integrates an input signal, so its output passes a threshold voltage established with a comparator and a voltage reference. Within the modulator, the analog-input signal is subtracted from the output of a 1-bit digital-to-analog converter (DAC). The DAC converter is part of the negative feedback loop. This differenced signal is converted by the integrator to a voltage that ramps from negative to positive or positive to negative, depending on the output of the difference amplifier.

This ramp is presented to one of the two inputs of a comparator. When the output of the integrator passes the reference voltage of the comparator, the output of the comparator toggles between high and low. On a regular time schedule, that output is fed back to the difference amplifier via the 1-bit DAC. Additionally, the output of the comparator is fed forward to a digital filter. With time, the output of the digital filter provides a multibit conversion result. This basic design topology has been used to create myriad Δ - Σ -based converters that provide high resolution for very small signals, such as those from a bridge sensor. Still, the challenge is



1. The first order Δ - Σ ADC can be represented by a modulator and a digital filter. Using this topology, a variety of high-resolution ADCs can be built for small signals from sources like bridge sensors.

implementing the modulator in a microcontroller.

The circuit in Figure 2 implements such a classical first-order Δ - Σ ADC using a single-supply CMOS operational amplifier, RC network, and an 8-bit PIC16C622 MCU. In this design, the integrator is implemented with the capacitor CINT. The current through R_1 is generated by V_{IN} and the current through R_2 is generated by V_{RA3} . These provide the currents

that charge the C_{INT} . Their combination charge or discharge C_{INT} to the point where the comparator output is toggled. By driving RA3 in accordance with the output of the comparator, C1_{OUT}, the 1-bit DAC can be implemented in firmware. At the same time, the digital filter can be realized with two counters, along with a simple averaging algorithm in firmware.

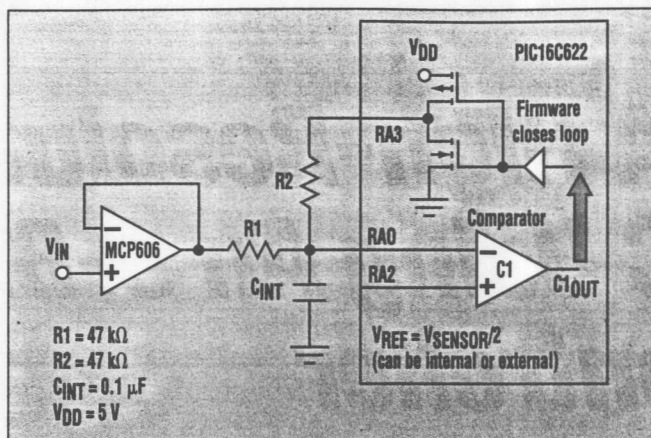
The absolute accuracy of this integrating capacitor isn't critical, but its stability from integration to integration is important. Because the capacitor voltage is held at a constant level in this circuit, the dielectric absorption of the capacitor isn't an issue. In this example, the maximum-voltage deviation due to the nonlinearity of the RC network is about 8 mV. If the RC time constant of the circuit is greater than the sample frequency, then the logarithmic nature of the time response will cause linearity errors in the system. The RC time-constant linearity error is minimized with:

$$t_{RC} = R1 \parallel R2 \times C_{INT}$$

$$t_{RC} \leq t_{SAMPLE}/10 \text{ (for good linearity)}$$

Capacitor leakage errors also will contribute to the system's overall error. The capacitor types that have appreciable leakage are the electrolytic ones. These include aluminum and tantalum, which shouldn't be used in this circuit. A capacitor type that fits well is the NPO ceramic type, due to its lower cost, smaller size, better stability, and wider range of values.

When V_{RA3} of the microcontroller is set high, the voltage at RA0 ramps up until the output of the comparator is triggered low. With the change in the compara-



2. The microcontroller's analog peripherals are combined with an external integrator to implement a first-order Δ - Σ modulator. The modulator is followed by a digital filter, also implemented by the 8-bit microcontroller, to realize a 10-bit Δ - Σ ADC.

tor output, the driver to the RA3 output is switched from high to low. With the potential at RA3 low, the capacitor starts to discharge, thereby causing the voltage at the input to the comparator (RA0) to decrease. The status of the output of RA3 remains low until the comparator is tripped high. Change in comparator output is clocked to the output of RA3 by the microcontroller.

The ratio of R1 and R2, with respect to the input-voltage range, are selected using the following formulas:

$$V_{IN(CM)} = V_{REF}$$

$$V_{IN(P-P)} = V_{RA3(P-P)} \times (R1/R2)$$

where: $V_{IN(CM)} = [(V_{IN(MAX)} - V_{IN(MIN)})/2 + V_{IN(MIN)}]$
 V_{REF} is the voltage applied at the

comparator's noninverting input. This voltage can be supplied internally by the microcontroller, or externally through the reference pin RA0.

$$V_{IN(P-P)} = (V_{IN(MAX)} - V_{IN(MIN)})$$

$$V_{RA3(P-P)} = (V_{RA3(MAX)} - V_{RA3(MIN)})$$

The low-offset, 25- μ A MCP606 CMOS op amp driving R1 is used to isolate errors that would be caused by the source impedance of the input signal. The op amp's offset voltage is 250 μ V at room temperature.

During the time that the modulator section of the circuit is cycling, two counters are used to keep track of the time, "Counter," and the total number of times that the comparator is high, "Result" (Fig. 2 again). The flow chart labeled DelSigA2D shows the algorithm employed to implement such a concept (Fig. 3).

When a conversion isn't in process, the output of the comparator is directly connected to RA3. This keeps the voltage at RA0 equal to the reference voltage of the comparator. When function DeltaSigA2D is called to perform a conversion, the result and counter variables are cleared (see the Code Listing, p. 118). Then, the comparator output is put under active program control.

The microcontroller program checks the output of the comparator at the beginning of each loop. If the voltage on the capacitor is less than the reference voltage (V_{RA2}), then the voltage at RA3 is set high. This injects charge onto the capacitor, C_{INT} , which increases the voltage at V_{RA0} . If the voltage on the capacitor is greater than the comparator's reference voltage, RA3 is set low, which removes the charge from the top of the capacitor. When the voltage at RA0 is greater than the voltage at RA2, the result register is incremented.

After this firmware decision, the counter register is incremented. This continues for as long as it's necessary to achieve the required resolution. For instance, ten bits of resolution requires 2^{10} (1024) times through the loop. Each

Parameter	Specification
Material	Carbon Fiber
Length	1.5m
Width	0.5m
Height	0.2m
Weight	15kg
Power Consumption	5W
Operating Temperature	-20°C to 60°C
Storage Temperature	-40°C to 85°C
Humidity	10% to 90% RH
Vibration	0.5g to 2g
Shock	10g to 20g
IP Rating	IP67
Communication	Bluetooth, Wi-Fi, 4G LTE
Accuracy	±0.1mm
Resolution	0.01mm
Response Time	10ms
Calibration	Factory Calibration
Warranty	2 Years

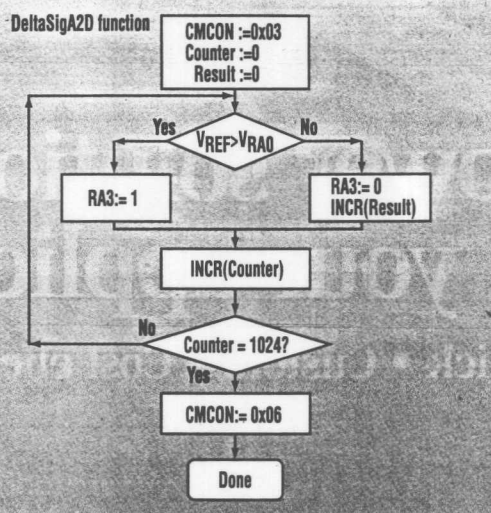
Rated capacity	32 oz (896 g)
Excitation	5 to 12 V dc
Rated output	2 mV/V $\pm$ 20%
Zero balance	$\pm$ 0.3 mV/V
Operating temperature	-55°C to 95°C
Compensated temperature	-5°C to 50°C
Zero balance over temperature	0.036% FS/°C
Output over temperature	0.036% FS/°C
Resistance	1200 Ω $\pm$ 300 Ω
Safe overload	150%
Full-scale deflection	0.01 to 0.05 in.

lap through the loop takes 17 instruction cycles. Additional no-operation (NOP) instructions are used to keep all paths through the code equal. Upon completion, the comparator output is fed directly to RA3, and the conversion is sent to output registers. If a PIC16C622 is used in this circuit with a 4-MHz clock, then the integration cycle will be 20 μ s. At this rate, the 10-bit conversion will take 20.48 ms.

Test data for this circuit shows that the maximum-code error was ± 2 counts, or 2 bits of uncertainty. Consequently, the effective number of bits in this ADC is 8 bits p-p (Fig. 4). This resolution can be improved by increasing the number of conversions and using digital filtering following these conversions.

Typically, a sensor that's configured as a Wheatstone bridge outputs a low-level differential signal. The design challenge for this type of a sensor is to capture these small signals and convert them into a digital format that provides an 8- to 12-bit representation. A circuit designed to capture these low-level voltages is depicted in Figure 5.

The analog portion of this circuit consists of the bridge sensor, an analog



3. This flow chart explains the algorithm employed to design a 10-bit ADC using a microcontroller integrated with analog functions like a comparator, voltage-reference, buffer, and output FETs. To achieve high performance, the designer must ensure that every conversion cycle through the flow chart is a constant.

multiplexer, an amplifier, and an RC network. The sensor that's selected for this example is a load cell. The rated output of the load cell is equal to 2 mV/V. When the bridge is excited with 5 V, the maximum-nominal output swing is equal to ± 10 mV. A complete

list of the load cell's specifications is provided by Table 1. The analog multiplexer is used to switch the two outputs of the sensor into the single-ended modulator. An amplifier configured as a buffer is used to isolate the sensor load from the modulator's RC network. This network implements the integrator function of a first order modulator.

The basic operation of this circuit is the same as the previous circuit with the exception of the multiplexer at the input. With this added feature, the two outputs of the Wheatstone bridge are alternately switched into the signal path after the counter register reaches 1024. The two results from these cycles are subtracted to give the conversion results. This technique provides 10 bits of resolution with 9.9 bits of accuracy (rms). Again, the design equations for this circuit are:

$$V_{IN(CM)} = V_{REF}$$

$$V_{IN(P-P)} = V_{RA3(P-P)} \times (R1/R2)$$

with:

$$V_{IN(CM)} \approx V_{DD}/2, \text{ or } (V_{LC+} + V_{LC-})/2$$

where V_{REF} is the voltage reference

Code Listing

```

*****
* Filename: DeltaSig.asm
*****
* Author: Dan Butler
* Company: Microchip Technology Inc.
* Revision: 1.00
* Date: 02 December 1998
* Assembled using MPASM V2.20
*****
* Include Files:
* p16C622.inc V1.01
*****
* Provides two functions implementing the Delta Sigma A2D.
* InitDeltaSigA2D sets up the voltage reference and comparator
* in the "idle" state.
* DeltaSigA2D runs the actual conversion. Results provided in
* result_l and result_h.
* See An700 figure 2 for external circuitry required.
*****
* What's changed
*****
* Date Description of change
*****
#include <p16C622.inc>
cblock
result_l
result_h
counter:2
endc

; *****
;
; InitDeltaSigA2D
; bcf STATUS,RP0
; movlw 0x0C
; movwf VRCON
; bcf PORTA,3 ;set comparator pin to output
; bcf STATUS,RP0
; movlw 0x06 ;set up for 2 analog comparators with common reference
; movwf CMCON
; return

; Delta Sigma A2D
; The code below contains a lot of nops and goto next instruction.

```

```

These
; are necessary to ensure that each pass through the loop takes the
; same
; amount of time, no matter the path through the code.
;
DeltaSigA2D
clrwf counter
clrwf counter+1
clrwf result_l
clrwf result_h
movlw 0x03 ; set up for 2 analog comparators with common reference
movwf CMCON
loop
btfsc CMCON,C1OUT ; Is comparator high or low?
goto complow ; Go the low route
comphigh
nop ; necessary to keep timing even
bcf PORTA,3 ; PORTA.3 = 0
incfsz result_l,f ; bump counter
goto eat2cycles ;
incf result_h,f ;
goto endloop ;
complow
bcf PORTA,3 ; Comparator is low
nop ; necessary to keep timing even
goto eat2cycles ; same here
eat2cycles
goto endloop ; eat 2 more cycles
endloop
incfsz counter,f ; Count this lap through the loop.
goto eat5cycles ;
incf counter+1,f ;
movf counter+1,w ;
andlw 0x04 ; Are we done? (We're done when bit2 of
btfsc STATUS,2 ; the high order byte overflows to 1).
goto loop ;
goto exit
eat5cycles
goto 5+1 ; more wasted time to keep the loops even
nop ;
goto loop ;
exit
movlw 0x06 ; set up for 2 analog comparators with common reference
movwf CMCON
return
end

```

applied to the comparator's noninverting input and is approximately $V_{\text{SENSOR}}/2$. If it's made external, this reference voltage can be used to adjust offset errors. Again:

$V_{\text{IN (P-P)}} = (V_{\text{LC+ (MAX)}} - V_{\text{LC+ (MIN)}})$,
OR $(V_{\text{LC+ (MIN)}} - V_{\text{LC- (MAX)}})$, which
equals the sensor's full scale range,
and:

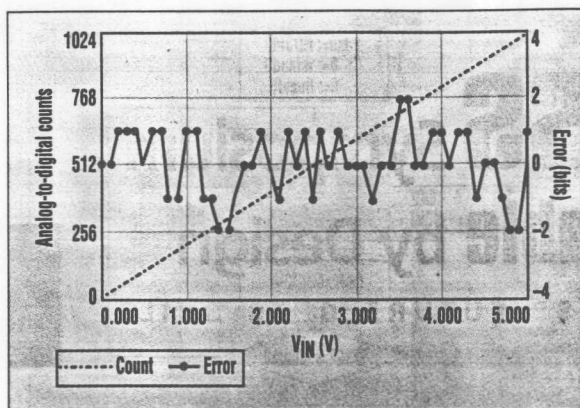
$$V_{\text{RA3 (PK-PK)}} = (V_{\text{RA3 (MAX)}} - V_{\text{RA3 (MIN)}})$$

The offset and gain are the dominant types of errors that the bridge and signal-conditioning path produces. Bridge sensor circuits also produce other errors, such as linearity, noise, hysteresis, repeatability, stability, and aging. But, these topics are beyond the scope of this article.

Mathematically, the offset error of a system can be described using the generic formula $\text{out} = a + bx$, where a is the offset error, b is the span or gain of the system, and x is the input to the system. In this equation, the offset error is described with a constant additive to the entire transfer function. The offset error is typically measured when the input signal is zero. This technique provides an output signal that's equal to the offset. The offset error can originate at the sensor or within the various components in the analog-signal path. This error is repeatable and stable unless the operating conditions—such as temperature, voltage excitation, or current excitation—change.

The offset errors in the circuit shown in Figure 5 come from the load cell, the operational amplifier (A1), the port leakage current at RA0, the comparator's voltage reference (V_{REF}), the comparator offset, and the nonsymmetrical output port of RA3. Half of the bridge-offset error is seen on the two output terminals of the bridge. Because the signal path for the two outputs of the sensor to the microcontroller are the same, the conversion data taken from the positive leg of the load-cell sensor (LC+) has the same signal-path offset and gain errors as the conversion data taken from the negative output of the load-cell sensor (LC-).

To accommodate these errors, the design equations for the circuit remain:



4. Test results indicate that the maximum-code error or uncertainty for the circuit in Figure 2 was 2 bits. Consequently, the effective number of bits for this ADC is 8 bits (p-p), or 9.9 bits (rms).

$$V_{\text{IN (CM)}} = V_{\text{REF}}$$

$$V_{\text{IN (P-P)}} = V_{\text{RA3 (P-P)}} \times (R1 / R2)$$

But, now the worst case variation is:

$$V_{\text{IN (P-P)}} = (V_{\text{LC+ (MAX)}} - V_{\text{LC+ (MIN)}}) +$$

$$LC_{\text{OFFSET}} + A1_{\text{OFFSET}} + RA0_{\text{OFFSET}} +$$

$$V_{\text{REF (OFFSET)}} + C1_{\text{OFFSET}} + RA3_{\text{OFFSET}}$$

where LC_{OFFSET} is the maximum-offset voltage that can be generated by the load-cell bridge, $A1_{\text{OFFSET}}$ is the offset voltage of the op amp, and $RA0_{\text{OFFSET}}$ is the offset error caused by the leakage current of port RA0. This leakage current is specified at 1 nA at room temperature and 0.5 μ A (max) over temperature. Plus, it causes a voltage drop across the parallel combination of R1 and R2. $V_{\text{REF (OFFSET)}}$ is the offset error of the internal voltage reference of the microcontroller. This error can be reduced significantly with an external voltage reference. Likewise, $C1_{\text{OFFSET}}$ is the offset of the internal comparator of the microcontroller and $RA3_{\text{OFFSET}}$ is caused by

the inability of RA3 to go completely to the rails. It can be quantified by $RA3_{\text{OFFSET}} = [(V_{\text{DD}} - RA3_{\text{HIGH}}) - RA3_{\text{LOW}}] / 2$. This formula assumes $V_{\text{REF}} = V_{\text{DD}} / 2$. The maximum magnitudes of these errors are summarized in Table 2.

The resulting offset errors are added to the differential-output voltage of the load cell. As a result, the output voltage for this system can be written as:

$$V_{\text{OUT}} = V_{\text{LC+}} + LC_{\text{OFFSET}} + A1_{\text{OFFSET}} +$$

$$RA0_{\text{OFFSET}} + V_{\text{REF (OFFSET)}} +$$

$$C1_{\text{OFFSET}} + RA3_{\text{OFFSET}} - V_{\text{LC-}} -$$

$$A1_{\text{OFFSET}} - RA0_{\text{OFFSET}} - V_{\text{REF (OFFSET)}} -$$

$$C1_{\text{OFFSET}} - RA3_{\text{OFFSET}}$$

which simplifies to:

$$V_{\text{OUT}} = V_{\text{LC+}} - V_{\text{LC-}} + LC_{\text{OFFSET}}$$

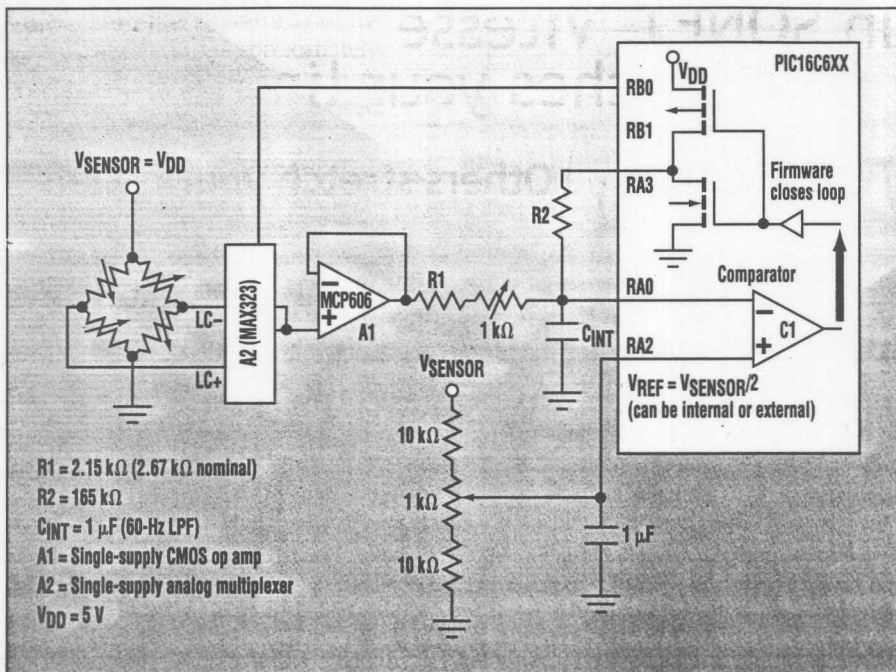
Given the design equations for this circuit and the errors in Table 2, the total expected offset error over temperature for the electronics is 67.8 mV. With a sensor full-scale range of ± 10 mV, the dynamic range of the system would be approximately 7.8 times larger than the nominal, error-free peak-to-peak range at the input of the comparator.

The 1-k Ω potentiometer with its wiper connected to RA0 is placed in series between the power supply (5 V) with two 10-k Ω , 1% resistors (Fig. 5 again). This configuration provides a voltage-reference range to the comparator of ± 19 mV centered around midsupply. If an external reference is used with a ± 0.5 -mV error range, the electronics will contribute ± 19.3 -mV offset error over temperature. This changes the worst-case full-scale peak-to-peak range of the system to ± 29.3 mV. This is only approximately three times larger than the nominal full-scale output (± 10 mV) of the sensor.

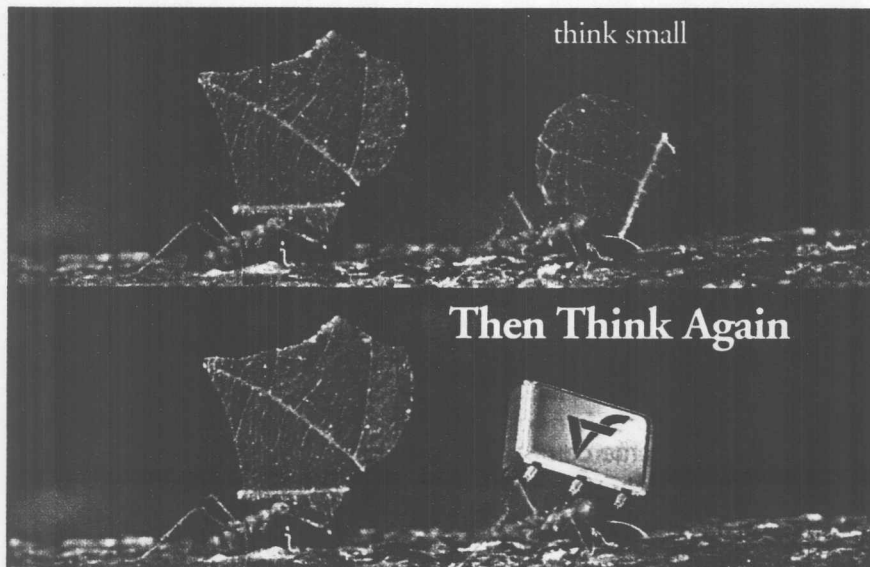
Offset errors of the circuit can be calibrated in firmware. This is performed by subtracting the conversion code results of LC+ from the results LC-. Firmware calibration is an efficient way to eliminate most of the offset errors. The tradeoff, however, for having offset adjustments performed by the microcontroller is dynamic range. In anticipation of these offset errors, the designer should increase the peak-to-peak analog-input range of the conversion system.

TABLE 2: SOURCES CONTRIBUTING OFFSET ERRORS IN FIG. 5

Error source	Offset voltage over temperature
Load cell bridge	± 1.5 mV in a 5-V system
Op amp	± 500 μ V
Port leakage, RA0	± 1.3 mV
Internal V_{REF}	± 49 mV
Comparator	± 10 mV
Output port, RA3 (asymmetrical output swing)	5.5 mV



5. Using the basic concept, a practical circuit is realized to measure voltage across a bridge sensor. Because the Wheatstone bridge provides two outputs, a multiplexer is used in front of the buffer to alternately switch the two outputs into the signal path of the ADC. The resistors have been selected to provide a $\pm 40.5\text{-mV}$ full-scale input range to the comparator. Given 9.9-bit (rms) accuracy, the LSB for this system is 84.7 μV .



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While this will result in a conversion that has a wider dynamic range, the accuracy of the system will be lower.

The span or gain of a system can be mathematically described as a constant, which is multiplied against the input signal. A system with a gain error deviates from the ideal, as described in the formula below:

$$\text{Actual output} = \text{Input} \times \text{Ideal gain} (1 + \text{Gain error})$$

For this circuit, the span errors are less influential than the offset errors. Additionally in Figure 5, the system span errors of the circuit originate in the load cell ($\pm 20\%$), the resistors ($\pm 1\%$), capacitor ($\pm 10\%$), and the on-resistance of the RA3 port (0.2%).

Span errors can be effectively removed in the analog domain. For instance, the span error of the sensor can be adjusted with the sensor's excitation voltage. As a tradeoff for this adjustment strategy, the common mode voltage of the sensor is changed, which creates offset errors with respect to the reference voltage (V_{REF}) of the comparator. This problem can be alleviated by making the voltage reference ratiometric to the sensor excitation source. Span errors also can be adjusted with either R1 or R2. A potentiometer is used to perform this function. This type of adjustment doesn't change the offset error of the system. The circuit is able to rely on firmware calibration with a reduction in the dynamic range of the system.

In reality, an alternative circuit has been proposed to perform the analog-to-digital conversion for slow-moving signals from sensors. This alternative is a low-cost and low-part-count solution that gives a high degree of resolution when the power of the microcontroller is used to implement digital filtering. ∇

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Recommended Reading:

Baker, Bonnie C., "Anti-aliasing, Analog Filters For Data-Acquisition Systems," AN699, Microchip Technology Inc.

Morrison, Ralph, *Noise and Other Interfering Signals*, John Wiley & Sons Inc., 1992.